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09/542,783	04/04/2000	John Whitman	4294US(98-1208)	6870

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EXAMINER	
KEBEDE, BROOK	
ART UNIT	**PAPER NUMBER**
2823	

DATE MAILED: 05/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/542,783	WHITMAN ET AL.	
	Examiner	Art Unit	
	Brook Kebede	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 March 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-87* is/are pending in the application.

4a) Of the above claim(s) *18-87* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/6/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 2, 8, 9, 11, 16 and 17 are rejected under 35 U.S.C. 102(e) as being anticipated by Kikuchi et al. (US/6,278,153).

The rejection that set forth in the Office action that was mailed on December 1, 2004 is maintained and repeated herein below as record.

Re claim 1, Kikuchi et al. disclose a method for disposing a material on a semiconductor device structure comprising: providing a semiconductor device structure (see Fig. 6D) including a surface (23 24 25 26) and at least one recess (23a) formed in the surface; disposing the material (20) on the surface (23 24 25 26) so as to substantially fill at least one recess (23a) and the material (20) covering the surface having a thickness less than a depth of said at least one recess (23a) without subsequently removing the material (20) from the surface, an upper surface of at least a portion of said material (20) over or within said at least one recess being substantially planar (23 24 25 26) (see Figs. 6A-6D; 10A-10E and 13A-13E;).

Re claim 2, as applied to claim 1 above, Kikuchi et al. disclose all the claimed limitations including disposing the material so as to substantially fill the at least one recess without substantially covering said surface (see Figs. 6A-6D; 10A-10E and 13A-13E;).

Re claim 8, as applied to claim 1 above, Kikuchi et al. disclose all the claimed limitations including upon exposing the material disposed over an entirety of said semiconductor device structure to an etchant, the material covering said surface is substantially removed therefrom, while the material located in said at least one recess substantially fills said at least one recess (see Figs. 6A-6D; 10A-10E and 13A-13E).

Re claim 9, as applied to claim 1 above, Kikuchi et al. disclose all the claimed limitations including the limitation wherein said providing said semiconductor device structure comprises providing a stacked capacitor structure with said at least one recess comprising at least one container formed in an insulator layer of said stacked capacitor structure, said surface and said at least one container being lined with a conductive material (see Figs. 6A-6D; 10A-10E; 13A-13E)

Re claim 11 as applied to claim 1 above, Kikuchi et al. disclose all the claimed limitations including the limitation wherein said disposing the material comprises disposing a mask material over said semiconductor device structure (see Fig. 6A-6D; 10A-10E; 13A-13E).

Re claims 16 and 17, as applied to claim 1 above, Kikuchi et al. disclose all the claimed limitations including the limitation providing a semiconductor device structure having a surface with at least one dual damascene trench recessed therein and a layer of conductive material, with a non-planar surface disposed in said at least one dual damascene trench add at least partially covering sand surface and disposing a stress buffer over said layer of conductive material, said stress buffer having a substantially planar surface without removing material thereof following said disposing (see Figs. 14A-14D).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 3-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kikuchi et al. (US/6,278,153) in view of Yoshihara (US/6,117,486).

The rejection that set forth in the Office action that was mailed on December 1, 2004 is maintained and repeated herein below as record.

Re claims 3-7, as applied to claim 1 above, Kikuchi et al. disclose all the claimed limitations including the limitation applying the material to the surface of the semiconductor device structure spinning the semiconductor device structure (see Kikuchi et al. Figs. 6A-6D; 10A-10E and 13A-13E). However, Kikuchi et al. do not disclose decreasing a rate of the spinning while permitting the material to at least partially cure and gradually increasing the rate of the spinning.

Yoshihara discloses applying the material to the surface of the semiconductor device structure spinning the semiconductor device structure both decreasing rate of spinning and while allowing the material to cure gradually increasing the rate of spinning; exposing the material to a soft balling temperature ; spinning rate of 1000 and 100 rpm (see Figs. 10 and Col. 13, lines 25-44). As Yoshihara discloses the method provided forming of resist film on the semiconductor wafer at predetermined and uniform thickness.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to have provided Kikuchi et al. reference with spinning the semiconductor device structure both decreasing rate of spinning and while allowing the material to cure gradually increasing the rate of spinning as taught by Yoshihara because the method would have provided to form a resist film on the semiconductor wafer at predetermined and uniform thickness.

5. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kikuchi et al. (US/6,278,153) in view of Lin et al. (US/6,046,083).

The rejection that set forth in the Office action that was mailed on December 1, 2004 is maintained and repeated herein below as record.

Re claim 10, as applied to claim 9 above, Kikuchi et al. disclose all the claimed limitations including forming of stacked capacitor structure having conductive layer. Although it is well-known in the art Kikuchi et al. do not disclose doped HSG.

Lin et al. disclose providing said semiconductor device structure having a stacked capacitor structure with the surface and at least one container being lined, with doped hemispherical grain polysilicon (see Figs. 7 and 8).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to have provided Kikuchi et al. reference with doped HSG as taught by Lin et al. because the device performance would have been enhanced (see Lin et al. Col. 1, lines 59-67 through Col. 2, lines 1-14).

6. Claims 12-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kikuchi et al. (US/6,278,153) in view of Park et al. (US/6,326,282).

Re claim 12, as applied to claim 1 above, Kikuchi et al. disclose all the claimed limitations including the limitation except providing a shallow trench isolation structure with at least one recess comprising at least one trench formed in a surface of the shallow trench isolation structure.

Park et al. disclose forming of a shallow trench isolation structure with at least one recess comprising at least one trench formed in a surface of the shallow trench isolation structure in order to form an isolation region between the device elements (see Figs. 2B-2E).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to have provided Kikuchi et al. reference with shallow trench isolation structure as taught by Park et al. because the shallow trench isolation structure would have provided isolation region between device elements in the substrate.

Re claim 13, as applied to claim 12 above, both Kikuchi et al. and Park et al. in combination disclose all the claimed limitations including the limitation wherein said disposing the material comprises disposing a mask material over said shallow trench isolation structure (see Park et al. Figs. 2B-2E).

Re claim 14, as applied to claim 12 above, both Kikuchi et al. and Park et al. in combination disclose all the claimed limitations including the limitation wherein said providing

said shallow trench isolation structure comprises providing said shallow trench isolation structure with an insulator layer substantially filling said at least one trench and covering said surface see Park et al. Figs. 2B-2E).

Re claim 15, as applied to claim 14 above, both Kikuchi et al. and Park et al. in combination disclose all the claimed limitations including the limitation wherein said disposing the material comprises disposing a stress buffer over said insulator layer, said stress buffer having a substantially planar surface without removing material thereof following said disposing see Park et al. Figs. 2B-2E).

Response to Arguments

7. Applicants' arguments filed on March 7, 2005 have been fully considered but they are not persuasive.

Applicants argued that "Kikuchi does not expressly of inherently describe the surface of resist 20 is substantially planar..."

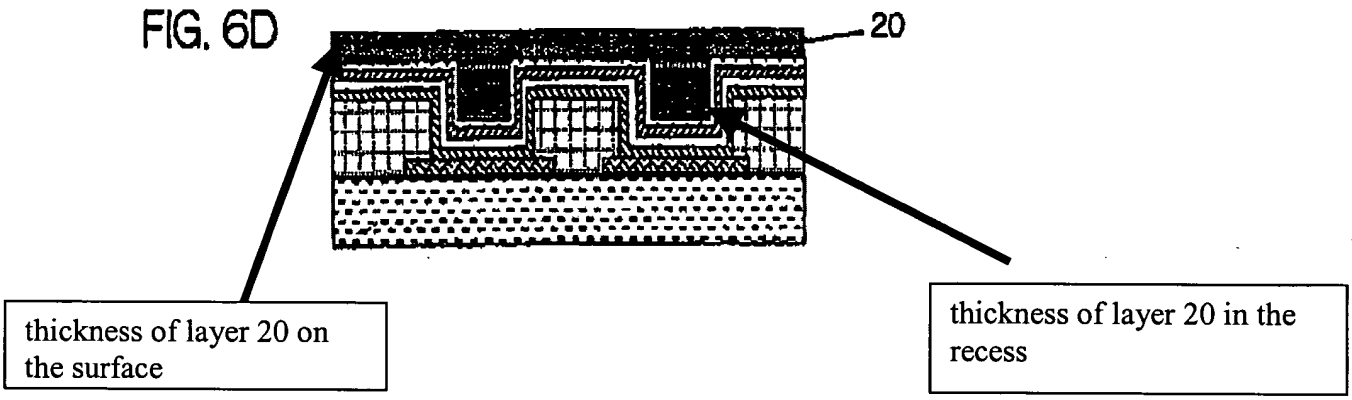
In response to applicants' argument, it is respectfully submitted that Kikuchi et al. '153 anticipates all the limitations of Claims 1, 2, 8, 9, 11, 16, and 17 of the instant application as applied in herein above.

With respect to claim l, Kikuchi et al. disclose a method for disposing a material on a semiconductor device structure comprising: providing a semiconductor device structure (see Fig. 6D) including a surface (23 24 25 26) and at least one recess (23a) formed in the surface; disposing the material (i.e., a resist layer) (20) on the surface (23 24 25 26) so as to substantially fill at least one recess (23a) and the material (20) covering the surface having a thickness less than a depth of the at least one recess (23a) without subsequently removing the material (20)

from the surface, an upper surface of at least a portion of said material (20) over or within the at least one recess being substantially planar (see Figs. 6A-6D; 10A-10E and 13A-13E; 16A-16F).

For example, as depicted in Fig. 6D below, Kikuchi et al. '153 clearly show the thickness

FIG. 6D



of layer **20** at the surface is lower than that of in the recess. Since there is no quantitative dimensional range in the rejected claims, appellants' argument that "Kikuchi et al. '153 drawings are not to scale" has no merit.

In addition, Fig. 6D shows a planar surface of the resist layer **20** on the surface which substantially fill the recess **23a**. Kikuchi et al. '153 also disclose in the specification spin-coating process, i.e., a well-known process to one having ordinary skill in the art to deposit resist layer and to planarize the layer, which by the way same process is used in the instant application for the purpose of achieving planar surface. The following disclosed by Kikuchi et al. '153: "as illustrated in FIG. 6D, resist 20 is deposited over the third electrically conductive thin layer **27**. If the resist **20** composed of liquid material, the liquid material is deposited on the third electrically conductive layer **27** by **spin-coating,** die-coating, curtain-coating or printing (see . Kikuchi et al. '153 Col. 17, lines 62-66). The purpose of spin-coating during

deposition of the resist layer, as well-known to one of ordinary skill in the art, is to form a resist layer having a planar surface. As the term implies, spin coating removes excess material as result of spinning of the wafer during coating operation. Therefore, Kikuchi et al. '153 as shown in Fig. 6D explicitly or implicitly teach depositing of a material **20** having planar surface on a surface.

Further, in response to applicants' argument that "As Kikuchi describes the use of a spin-coating process to introduce resist 20 into via-holes 23a, it is clear that the result of both the spin-coating process and the surface tension of the resist would be nonplanarity of the surface of resist 20 within the via-holes 23a. It is also respectfully submitted that Kikuchi lacks any inherent description that the method described therein results in a layer of resist 20 with a planar surface....," it is respectfully submitted that such conclusion by the appellants is based on mere speculation and misconstruction of Kikuchi et al. '153 reference because the there is nothing in claim 1 specifies quantitative or qualitative measurement for **degree of planarization**. In addition, claim 1 does not recite how **planarization** process is conducted that can be different form that of the Kikuchi et al. '153 reference. As a matter of fact, claim 1 recites "the material over or within the at least of one recess being substantially planar." Kikuchi et al. '153 disclose a substantial planar resist layer 20 as depicted in Fig. 6D that resulted form spin coating process (i.e., s similar process as of the spin coating process of the instant application).

In this case, claims are given their broadest reasonable interpretation in light of the supporting disclosure. See *In re Morris*, 127 F.3d 1048, 1054-55, 44 USPQ2d 1023, 1027-28 (Fed. Cir. 1997). Limitations appearing in the specification but not recited in the claim are not read into the claim. See *In re Prater*, 415 F.2d 1393, 1404-05, 162 USPQ 541, 550-551 (CCPA 1969). See also *In re Zletz*, 893 F.2d 319, 321-22, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989).

With respect to claim 2, applicants further argued that "Kikuchi neither expressly nor inherently describes *disposing* a material on a surface of a semiconductor device structure and within recesses thereof so as to substantially fill the recesses *without substantially covering* the *surface*, . . ."

In response to the appellants' argument, it is respectfully submitted that Kikuchi et al. '153 teach all the claimed limitations of claim 2.

In light of the supporting disclosure, claim 2 is interpreted in view of Figs. 2 and 3 of the instant application. For illustrative purpose, Figs. 2 and 3 are reproduced below.

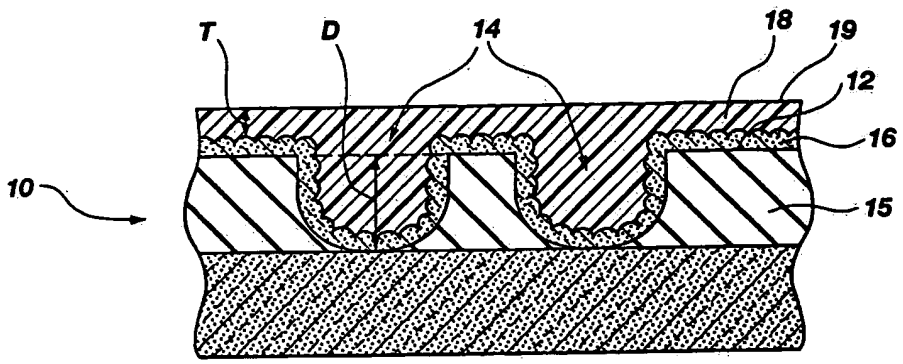


Fig. 2

As depicted in Fig. 2 above, the material layer **18** is disposed over a surface **12** to substantially fill the recess (container) **14** (see the instant application specification in Page 12, paragraph 0038). As recited in claim 2, "wherein said disposing comprises disposing said material so as substantially fill said at least one recess without substantially without substantially covering said surface" is interpreted in conjunction with Fig. 3. After the material layer **18** (i.e., the resist layer) deposited to fill the recess **14** and cover the surface **12** as sown in Fig. 2 above, the material layer **18** (i.e., the resist layer) is removed form the surface (i.e., *disposing* a material on

a surface of a semiconductor device structure and within recesses thereof so as to substantially fill the recesses *without substantially covering* the *surface*) during subsequent process as sown in Fig. 3 below (see also the instant application specification page 14, paragraph 0041).

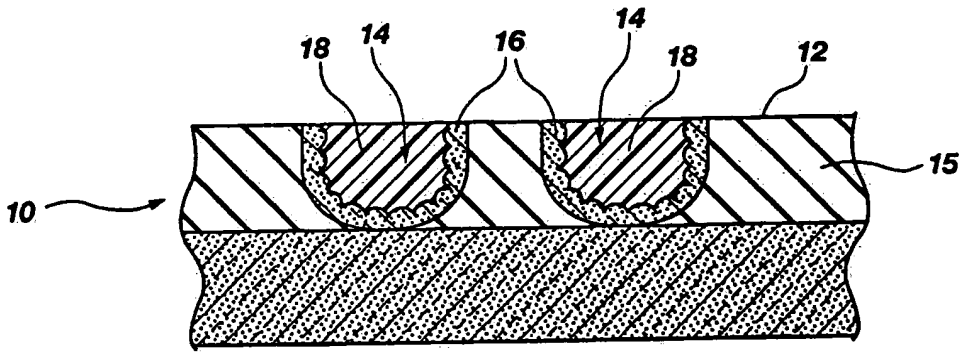


Fig. 3

In addition, there is no selective deposition process disclosed in appellants' disclosure or in the rejected claims that would lead one of ordinary skill in the art to a different interpretation.

Similarly, Kikuchi et al. '153 disclosure, as depicted in Figs. 6E and 6F or 16D-16F below, is consistent with claim 2 and Figs. 2 and 3 of the instant application.

FIG. 6E

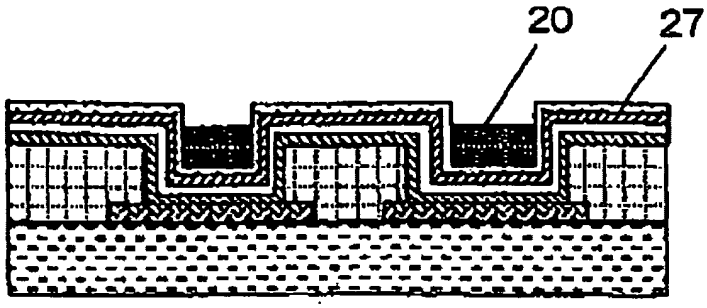


FIG. 6F

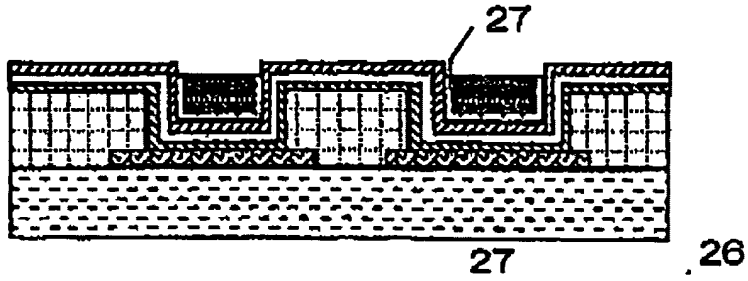


FIG. 16D

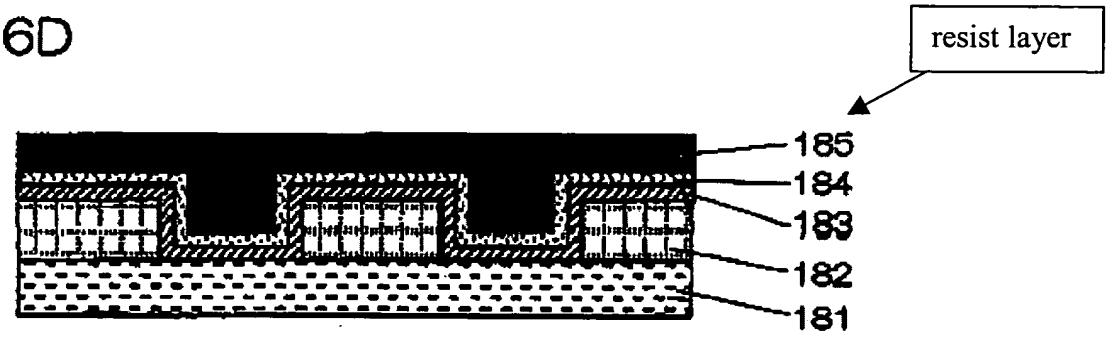


FIG. 16E

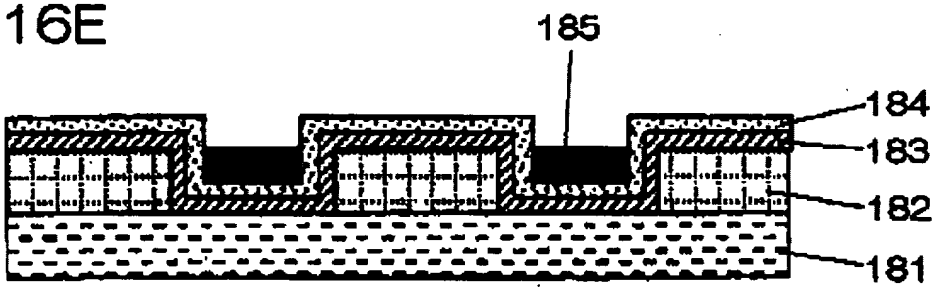
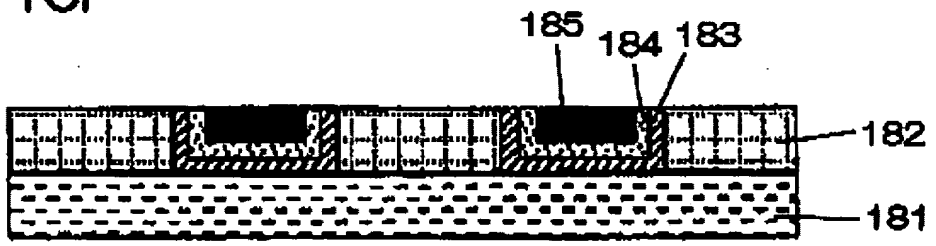


FIG. 16F



Hence, applicants' contention that "Kikuchi neither expressly nor inherently describes disposing a material on a surface of a semiconductor device structure and within recesses thereof so as to substantially fill the recesses without substantially covering the surface..." has no merit because the rejected claim is consistent with Kikuchi et al. '153 disclosure.

Furthermore, claims are given their broadest reasonable interpretation in light of the supporting disclosure. See *In re Morris*, 127 F.3d 1048, 1054-55, 44 USPQ2d 1023, 1027-28 (Fed. Cir. 1997). Limitations appearing in the specification but not recited in the claim are not read into the claim. See *In re Prater*, 415 F.2d 1393, 1404-05, 162 USPQ 541, 550-551 (CCPA 1969). See also *In re Zletz*, 893 F.2d 319, 321-22, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989).

Therefore, the rejection of claims 1, 2, 8, 9, 11, 16 and 17 under 35 U.S.C. § 102 is deemed proper.

With respect to applicants' argument of rejection of claims 3-7 under 35 U.S.C. 103, i.e., "neither Kikuchi, Yoshihara, nor knowledge available to one ordinarily skilled in the art would have motivated one of ordinary skill in the art to combine teachings from Kikuchi with teachings from Yoshihara to arrive at the inventions to which claims 3-7 are drawn...," it is respectfully submitted that the combination of Kikuchi et al. '153 and Yoshihara '486 teach all the limitations of Claims 3-7 of the instant application as applied in Paragraph 10(b) herein above.

The combination of Kikuchi et al. '153 and Yoshihara '486 discloses applying the material to the surface of the semiconductor device structure, spinning the semiconductor device structure and decreasing rate of spinning while allowing the material to cure gradually, and finally increasing the rate of spinning; exposing the material to a soft balling temperature; spinning rate of 1000 and 100 rpm (see Yoshihara '486 Figs. 10 and Col. 13, lines 25-44).

Both Kikuchi et al. '153 and Yoshihara '486 teachings are directed to coating of material (i.e., resist coating) on a substrate for the purpose of fabricating semiconductor device. Therefore, the teachings of Kikuchi et al. '153 and Yoshihara '486 are analogous. It would have been within the scope of ordinary skill in the art to combine the teachings of Kikuchi et al. '153 and Yoshihara '486 in order to modify spin coating process of Kikuchi et al. '153 by adjusting the spinning rate (rpm) according to the teachings of Yoshihara '486 because one having ordinary skill in the art would have been motivated to look to analogous art teaching alternative suitable or useful methods for spin coating process as disclosed by Yoshihara '486. In addition, the rational to combine (i.e., to form a resist film on the semiconductor wafer at predetermined

and uniform thickness) the references can be found in Yoshihara '486 Col. 13, line 26 - Col. 14, line 67. The strongest rationale for combining references is a recognition, expressly or impliedly in the prior art or drawn from a convincing line of reasoning based on established scientific principles or legal precedent, that some advantage or expected beneficial result would have been produced by their combination. See *In re Sernaker*, 702 F.2d 989, 994-95, 217 USPQ 1, 5-6 (Fed. Cir. 1983).

Therefore, the *prima facie* case of obviousness has been met and the rejection under 35 U.S.C. § 103 is deemed proper.

With respect rejection of claim 10 under 35 U.S.C. 103, i.e., "claim 10 should be allowable because claim 1 is allowable...," it is respectfully that such an argument is not convincing because claim 1 is not allowable for the reasons indicated above. It is respectfully submitted that the combination of Kikuchi et al. '153 and Lin et al. '083 teach all the limitations of Claim 10 of the instant application as applied in Paragraph 10(c) herein above.

Both Kikuchi et al. '153 and Lin et al. '083 teachings are directed to depositing semiconductor thin films over the semiconductor substrate for purpose of fabricating a semiconductor device, particularly, semiconductor stacked capacitor device. Therefore, the teachings of Kikuchi et al. '153 and Lin et al. '083 are analogous. It would have been within the scope of ordinary skill in the art to combine the teachings of Kikuchi et al. '153 and Lin et al. '083 in order to increase the surface area of the capacitance the capacitor of Kikuchi et al. '153 by using doped hemispherical grain polysilicon according to the teachings of Lin et al. '083. One having ordinary skill in the art would have been motivated to look to analogous art teaching alternative suitable or useful methods for increasing the surface area of the capacitor by utilizing doped hemispherical grain polysilicon as applied by Lin et al. '083.

Therefore, the *prima facie* case of obviousness has been met and the rejection under 35 U.S.C. § 103 is deemed proper.

Pertaining to applicants' argument with respect rejection of claims 12-15 under 35 U.S.C. 103, i.e., "claims 12-15 should be allowable because claim 1 is allowable...," it is respectfully submitted that the combination of Kikuchi et al. '153 and Park et al. '282 teach all the limitations of Claims 12-15 of the instant application as applied above.

Both Kikuchi et al. '153 and Park et al. '282 teachings are directed to fabricating a semiconductor active devices on a semiconductor substrate. Therefore, the teachings of Kikuchi et al. '153 and Park et al. '282 are directed to analogous art. It would have been within the scope of ordinary skill in the art to combine the teachings of Kikuchi et al. '153 and Park et al. '282 in order to provide isolation between different transistor or capacitor areas of Kikuchi et al. '153 by using the shallow trench isolation (STI) as taught by Park et al. '282 because one having ordinary skill in the art would have been motivated to look to analogous art teaching alternative suitable or useful methods for electrically isolating one device form another.

Therefore, the *prima facie* case of obviousness has been met and the rejection under 35 U.S.C. § 103 is deemed proper.

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Correspondence

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brook Kebede whose telephone number is (571) 272-1862. The examiner can normally be reached on 8-5 Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (571) 272-1855. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9306 for regular communications and (703) 872-9306 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571) 272-1950.

Brook Kebede
Examiner
Art Unit 2823

BK
May 10, 2005